Amorphous superconducting nanowire single-photon detectors integrated with nanophotonic waveguides

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M. Häußler,[1,2,3] M. Yu. Mikhailov,[4] M. A. Wolff,[1,2,3] and C. Schuck[1,2,3,a)]

AFFILIATIONS

[1] Institute of Physics, University of Münster, Wilhelm-Klemm-Str. 10, D-48149 Münster, Germany
[2] Center for NanoTechnology (CeNTech), Heisenbergstr. 11, D-48149 Münster, Germany
[3] Center for Soft Nanoscience (SoN), Busso-Peus-Str. 10, D-48149 Münster, Germany
[4] B. Verkin Institute for Low Temperature Physics and Engineering of the National Academy of Sciences of Ukraine, 61103 Kharkiv, Ukraine

[a)] **Author to whom correspondence should be addressed:** carsten.schuck@uni-muenster.de

ABSTRACT

Future applications in integrated quantum photonics will require large numbers of efficient, fast, and low-noise single-photon counters. Superconducting nanowire single-photon detectors made from amorphous material systems are best suited to meet these demands, but the integration with nanophotonic circuits has remained a challenge. Here, we show how amorphous molybdenum silicide (MoSi) nanowires are integrated with nanophotonic silicon nitride waveguides in traveling wave geometry. We found a saturated on-chip detection efficiency of (73 ± 10) % for telecom wavelength photons and the sub-10 Hz dark count rate at a temperature of 2.1 K, which allows for operation in robust, compact, and economic cryogenic systems. Applications requiring fast counting will benefit from the sub-5 ns recovery times of our devices that we combine with 135 ps timing accuracy. Achieving this performance with waveguide-integrated amorphous superconductors is an important step toward enabling high yield fabrication of competitive single-photon detectors on a large variety of nanophotonic material systems.

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Superconducting nanowire single-photon detectors (SNSPDs) offer distinguished measurement capabilities in modern quantum technology applications such as quantum communication,[1,2] quantum simulations,[3] and quantum sensing.[4,5] The advantages of SNSPDs over other single-photon detector technologies are their superior detection efficiency from the UV to mid-IR wavelengths, low noise performance, high speed, and timing accuracy.[6] While conventional SNSPDs are typically illuminated under normal incidence from an optical fiber, SNSPDs can also be integrated with nanophotonic waveguides in traveling wave geometry, where photons are absorbed in a nanowire along their direction of propagation.[7–9] Such waveguide-integrated SNSPDs hold great promise for fully integrated, scalable quantum photonic circuits on silicon chips and may even become attractive stand-alone detector solutions with efficient fiber-to-waveguide coupling strategies.[10,11]

Waveguide-integrated SNSPDs have been realized on a small number of distinguished material platforms in various geometries, targeting a growing number of functionalities.[12–16] These realizations exclusively rely on crystalline or polycrystalline nanowire materials, predominantly niobium nitride (NbN) and niobium titanium nitride (NbTiN), with relatively high critical temperatures. However, to fully leverage the potential of SNSPDs for integrated quantum technology, future applications demand larger numbers of detectors and a wider range of nanophotonic material systems, e.g., for exploiting nonlinear optical effects.[17,18] This can be achieved with amorphous material systems, such as tungsten silicide (WSi), showing superior performance in terms of detection efficiency[19]

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and device yield[20,21] in conventional fiber-coupled SNSPDs, while requiring more complex and costly cryogenic technology. Different from (poly-)crystalline superconductors, amorphous materials naturally require no matching to the substrate lattice structure[22] and allow for room-temperature deposition,[23] yielding thin films with homogeneous superconducting properties on various substrates. Several amorphous superconducting materials have previously been considered with regard to their suitability for single-photon detection.[24] For applications in nanophotonics, we consider molybdenum silicide (MoSi), a particularly interesting candidate, because promising performance in the telecom wavelength regime has recently been observed with the conventional meander-shaped MoSi-SNSPD at temperatures above 2 K,[25–30] which allows for operation in state-of-the-art cost-effective and stable cryogenic systems. Contrary to conventional SNSPDs, however, the integration of amorphous superconducting nanowires with nanophotonic waveguides poses extraordinary challenges both in the device design and fabrication. On the one hand, the multi-layer design flows of nanophotonic devices with waveguide-integrated SNSPDs necessarily need to take into account a much larger number of free parameters than previously required for realizing conventional amorphous SNSPDs, and on the other hand, amorphous material systems impose new constraints on the overall nanofabrication process that are not readily compatible with the established routines developed for nanophotonic applications. In the case of MoSi, for example, one observes that the electron beam patterning processes of nanowires and waveguides developed for crystalline superconductors[7,12–16,31] have a detrimental effect on SNSPD performance. These limitations have prevented the integration of highly performing detectors made from amorphous thin films with fully functional nanophotonic circuits, instead only basic functionalities could be realized at operating temperatures below 1 K.[32–35]

Here, we show how these limitations can be overcome for amorphous MoSi-SNSPDs integrated with nanophotonic silicon nitride (Si_3N_4) waveguides on a silicon chip. We implement a novel nanophotonic fabrication process that yields highly performing waveguide-integrated SNSPDs operating at temperatures above 2 K. We show high detection efficiency for telecom wavelengths photons guided in SiN-on-insulator waveguides that are well-suited for future implementations of large-scale photonic circuits requiring large numbers of detection channels. Our devices further show low dark count rates (DCRs), high operating speed, and good timing accuracy. Notably, these performance benchmarks are achieved at an operating temperature of 2.1 K in a closed-cycle 4He cryostat. Demonstrating these characteristics with an amorphous superconductor constitutes the first step toward integrating SNSPDs with nontraditional waveguide material systems as well as tackling the yield challenge that currently prevents the realization of photonic circuits with large numbers of detection channels, as required for photonic quantum simulations and multi-channel quantum key distribution systems.

The fabrication of amorphous SNSPDs integrated with nanophotonic circuits starts with depositing MoSi-thin films by dc magnetron co-sputtering from molybdenum and p-doped silicon (resistivity of 2 Ω × cm) targets in an Ar plasma on 340 nm LPCVD SiN-on-insulator wafers. Substrates were mounted on a rotating holder held at room-temperature during deposition. After deposition of a 3.2 nm thin amorphous Si buffer layer, we sputter a 4.2 nm thin MoSi film, which is immediately capped with another 3.2 nm thin amorphous Si layer. We determine the MoSi film thickness from the ~4 Å/s deposition rate that was calibrated via high resolution transmission electron microscopy on witness samples. We further employ calibrated deposition rates of the atomic constituents to determine the film composition as $Mo_{68}Si_{32}$. X-ray diffraction studies confirm the amorphous structure of the films. The films show a critical temperature of T_c = 4.4 K and a square resistance of 390 Ω at room-temperature. A slightly reduced T_c in comparison to the highest reported T_c values for MoSi films of similar thickness[36–38] is the result of intentionally decreasing the Mo content in our films in order to reduce the superconducting gap with the goal of achieving increased quantum efficiency at elevated operating temperatures.

The realization of high-quality nanowires from MoSi thin films presents significant patterning challenges because the prevailing high-resolution negative-tone resist lithography processes, e.g., employing hydrogen silsesquioxane, show a detrimental effect on this amorphous superconducting material system. On the other hand, prior efforts with established positive-tone electron beam lithography resists for realizing isolated nanowires with sub-100 nm width, as desirable for high performance SNSPDs, had proven difficult.[26–28] Related attempts at realizing waveguide-integrated MoSi-SNSPDs have hence only resulted in devices that show a detector response when front side illuminated and lack photonic integrated circuit functionality.[35] We here overcome these challenges by using a multi-layer lithography process with high overlay accuracy that relies exclusively on CSAR6200 positive-tone resist for both nanowire and nanophotonic circuit patterning with high aspect ratios. After thin film deposition, we use electron beam lithography and physical vapor deposition of a 100 nm gold layer to produce electrode pads in a lift-off process. In a subsequent lithography step with a 1 nA electron beam, we define U-shaped nanowires of various lengths and widths employing CSAR6200.04 resist (Allresist) for optimal resolution and aspect ratio. Prior to development in an amyl acetate based solvent mixture (AR 600-546), we apply an additional electron beam exposure with 10 nA current in order to expose the CSAR6200.04 resist covering areas in which waveguide-structures are to be patterned in the subsequent nanophotonic layer as well as around the contact pads for electrical isolation. The corresponding pattern is then transferred into the underlying MoSi layer via reactive ion etching in an SF_6/Ar plasma. The photonic circuitry is fabricated in a final electron beam lithography step, which is precisely aligned to the previously patterned nanowires. Here again, we use positive-tone resist (CSAR6200.13, Allresist), completely encapsulating the MoSi-nanowires, in order to pattern nanophotonic structures, including grating couplers, waveguides, and power splitters. Reactive ion etching in fluorine chemistry then transfers the nanophotonic pattern to the 340 nm thick SiN-layer. On a half-inch by half-inch sized chip, we fabricate 400 devices with varying nanowire and nanophotonic circuit component dimensions in order to sample the large design parameter space and enable experimental identification of optimal performance parameters. As shown in Fig. 1, the resulting devices allow for electrical and optical access to MoSi-nanowires via the Au-electrodes and grating couplers that route light to SNSPDs via low-loss waveguides, respectively. The design of the nanophotonic circuit was optimized for facilitating precise determination of the photon flux arriving

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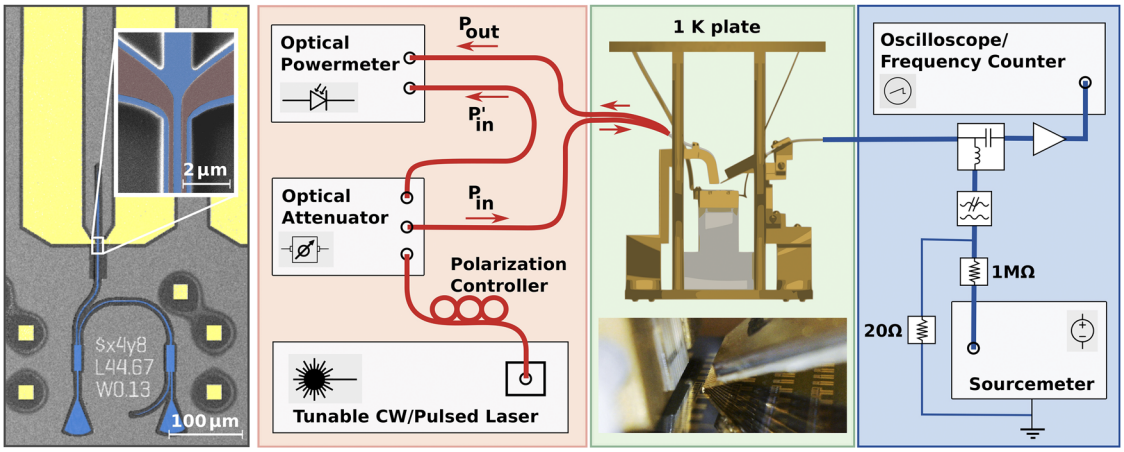

FIG. 1. Left: False color scanning electron micrograph of a single detector device with nanophotonic structures (blue) for optical access to the detector and calibration as well as gold electrodes (yellow) for supplying bias current and electrical readout. The inset shows the MoSi nanowire buried under resist (red) on top of the waveguide. Note that due to the positive-tone resist based lithography process, the photonic structures and electrical contact pads are surrounded by the remaining superconducting thin film, separated by a 5 μm–10 μm wide clearance region to prevent undesired optical loss in the photonic integrated circuit and guarantee electrical isolation, respectively. Right: Schematic measurement setup consisting of the optical input and readout (red), the chip with optical and electrical access on a sample holder inside the cryostat (green), and the electrical bias and readout circuit (blue).

at the detector via transmission measurements similar to previous work.[39]

The waveguide-integrated SNSPDs are characterized in a closed-cycle cryostat that achieves temperatures of 2.1 K at the chip in continuous operation. The cryogenic measurement setup allows for optical access to the chip via a single-mode fiber array that connects to telecom C-band lasers via calibrated optical attenuators and polarization controllers, as shown in Fig. 1. We use low-temperature compatible nanopositioners to align the grating couplers on a chip with respect to the optical fibers in the array and calibrate the number of photons arriving at the waveguide-integrated detector via transmission measurements using a reference output port in an established procedure.[40] Once optical access to a device is established, we gain electrical access to the electrodes on the chip via a radio-frequency (rf) probe, which we then use to supply bias current from a low-noise sourcemeter to the SNSPDs (see Fig. 1). We read out the electrical response from an SNSPD with a bias-T and low-noise amplifiers at room-temperature that allow us to register output pulses on an oscilloscope or a universal frequency counter. To prevent latching of the SNSPDs, we connect a resistor, R_p, in parallel to the detector outside of the cryostat, i.e., at room-temperature.[41] We determine the bias currents for our SNSPDs from the output current supplied by the sourcemeter and taking into account both the parallel resistance, $R_p = 20\ \Omega$, and the resistance of the wire to the detector, $R_w = 35\ \Omega$, including contact resistances. For typical waveguide-integrated MoSi-SNSPD devices, we find critical current densities of 0.9 MA/cm^2, similar to previous reports on current-biased MoSi-nanowires,[27] thus indicating that our fabrication process indeed caused minimal device damage.

We assess the electrical and optical performance of several devices on a chip in the key detector benchmarking disciplines of detection efficiency, dark count rate, detector reset time, and timing accuracy. Within the considered parameter range, we find the optimal all-around detector performance for nanowire geometries of 90 nm width and 80 μm length with critical currents of up to 3.3 μA. When 1550 nm wavelength photons from a continuous-wave telecom laser are incident on the detector, i.e., propagating inside the SiN-waveguide below the MoSi-nanowire, we observe an increase in the on-chip detection efficiency (OCDE) with the bias current applied to the nanowire, as shown in Fig. 2. Notably, the on-chip detection efficiency reaches saturation at bias current values of about 80% of the device critical current, corresponding to 2.6 μA. For rates up to 10 MHz of photons arriving at the detector, we observe a saturation plateau at a maximal on-chip detection efficiency of (73 ± 10) %. We note that the error increases significantly very close to the critical current, making the calculation of the on-chip detection efficiency unreliable. The larger uncertainty is a result of the exponential increase in the dark count rate, which necessarily needs to be determined in an independent measurement under slightly different conditions, e.g., temperature. The data presented in Fig. 2 therefore underestimate the actual detection efficiency of our device over the bias current range where the dark count rate becomes comparable to the incident photon flux. Nonetheless, the observed saturation of the detection efficiency extends well into the regime of the negligible dark count rate, i.e., at lower bias currents, and indicates that the internal quantum efficiency saturated at values larger 80%.[42,43] The overall detection efficiency, however, also depends on the efficiency with which photons in the waveguide are absorbed by the MoSi-nanowire, which is independent of bias current. For an 80 μm long nanowire, we expect an absorption efficiency of 85%, i.e., 0.096 dB/μm, which we determine from a fit to the experimental data acquired in independent measurements at cryogenic temperatures on reference devices located on the same chip (see the inset of Fig. 2). While these data are in agreement (i.e., within error bars), differences between the measured and expected on-chip detection efficiency in the plateau region may occur due to slight variations in the

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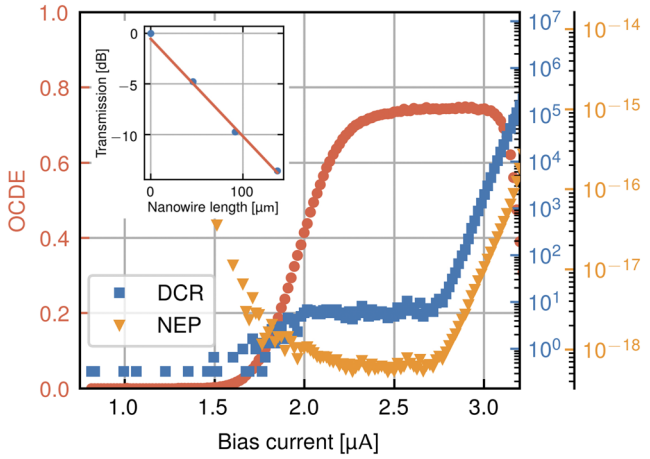

FIG. 2. On-chip detection efficiency (OCDE, red), dark count rate (DCR in 1/s, blue), and noise equivalent power (NEP in W/$\sqrt{\text{Hz}}$, orange) for a 90 nm wide, 80 μm long MoSi-SNSPD at 2.1 K, receiving a flux of 100 kHz telecom wavelength photons. A plateau region indicates saturated internal detection efficiency. The inset shows the experimental data (blue) and an exponential fit (red) of the light transmitted through SiN-waveguides covered with 90 nm wide U-shaped nanowires of different lengths.

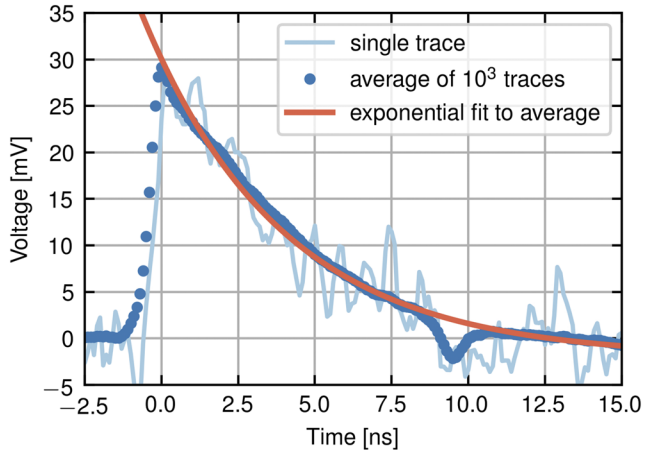

FIG. 3. Electrical response of an 80 μm long SNSPD at a bias current of 2.6 μA. From the exponential fit (red) to the data (blue), we find a decay time of 4.6 ns. The feature at 9 ns results from a back-reflection at the amplifiers in the electrical readout circuit.

width of the nanowires used for measuring the detection efficiency and the absorption efficiency, which we determine via scanning-election microscopy. We further find sub-10 Hz dark count rates (DCRs) within the bias current range, showing saturated detection efficiency, as shown in Fig. 2. The DCR was measured under regular operating conditions, resulting in stray light guided from the laboratory through the fiber into the cryostat and onto the detector. We expect the intrinsic DCR of the detectors to be two orders of magnitude lower than the DCR we measured under regular operating conditions.[19,42,44] Operating the SNSPD in the saturation regime thus allows for achieving a noise equivalent power of 5×10^{-19} W/$\sqrt{\text{Hz}}$ for photons in a nanophotonic waveguide, which is beneficial for realizing integrated sensing applications at the single-photon level.

We further assess the recovery time of our MoSi-SNSPDs, which is indicative of the maximum achievable count rate. This time interval that a nanowire requires to reset the superconducting state after a photon detection event closely approaches the decay time of an electrical output pulse from the SNSPD. We hence record the electrical response at a bias current of $I_b = 2.6\ \mu$A for a large number of detection events on a 3 GHz oscilloscope and observe the averaged pulse shape shown in Fig. 3. An exponential fit to the data yields a decay time of $\tau = 4.6$ ns for the 80 μm long and 90 nm wide nanowire. The decay time also allows for extracting the kinetic inductance of the nanowire, $L_k = \tau \cdot R_L$, where $R_L = 50\ \Omega$ is the load resistance of the readout circuit. We hence find $L_k = 230$ nH for the nanowire considered here, corresponding to a kinetic inductance per square of 257 pH, in good agreement with values reported recently for MoSi-SNSPDs fabricated from 4 nm to 6.6 nm thin films of slightly different material composition.[26,27]

Finally, we evaluate the timing accuracy of our waveguide-integrated MoSi-SNSPDs by determining the jitter performance of their electrical response on a 3 GHz oscilloscope. We use a pulsed telecom wavelength laser producing 1 ps short pulses at a repetition rate of 40 MHz and attenuate the output to the single-photon level, i.e., when incident on the SNSPD. The jitter of the pulsed laser was measured independently to be below 3 ps, which in our case only constitutes a minor contribution to the measurement of the overall detector jitter. We then measure the time interval between the laser synchronization output, derived from a fast internal photoreceiver, and the electrical response of our SNSPDs after amplification at room-temperature. Figure 4 shows a histogram of recorded time intervals at a bias current of 2.97 μA. From the full-width at

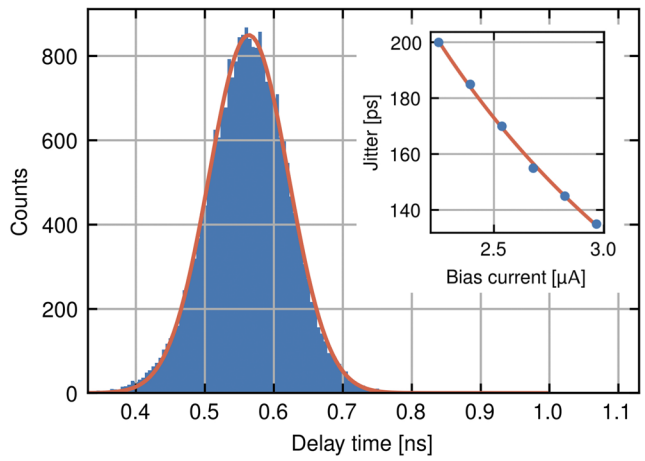

FIG. 4. Timing jitter measured at a bias current of 2.97 μA for an SNSPD of 90 nm width and 80 μm length. A 135 ps FWHM was extracted from a Gaussian fit (red) to the data (blue). Inset: Bias current dependence of the detector jitter. A large electrical jitter is observed at low absolute bias currents due to the low signal-to-noise ratio of the SNSPD output pulses.

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TABLE I. Comparison of performance characteristics of the state-of-the-art waveguide-integrated SNSPDs including nanowire thickness T, width W, length L, operating temperature T_{op}, and critical current I_c.

Platform	OCDE (%)	τ	DCR (cps)	Jitter (ps)	T (nm)	W (nm)	L (μm)	T_{op} (K)	I_c (μA)	Comment
NbN/SiN[46]	68	3 ns	...	60	4	80	140	1.6	...	U-shape
	86	10 ns	~50	56	4	80	240	1.6	11	W-shape
NbN/Si[39]	67	480 ps	<0.1	29	4	80	3	1.6	16	PhC cavity
NbTiN/SiN[47]	...	...	...	23	9.5	70	50	4.2	11.6	Series inductor
WSi/SiN[32]	...	~10 ns	<1	...	3.5	250	200	0.7	4.7	i-line litho
MoSi/SiN	73	4.6 ns	10	135	4.2	90	80	2.1	3.3	This work

half maximum (FWHM) of a Gaussian fit to the histogram data, we extract a jitter value of 135 ps, similar to timing uncertainties reported for conventional amorphous SNSPDs operated at comparable bias currents.[19,27] We confirm the expected inverse proportionality of the jitter and bias current[45] in measurements over the 2.2 μA–3.0 μA bias current range, as shown in the inset of Fig. 4, which indicates that the jitter is limited by the electrical readout circuit, and not by intrinsic properties of the detector.

To benchmark our device against recent work on waveguide-integrated SNSPDs, we compare relevant performance characteristics in Table I.

We achieve on-chip detection efficiencies on a par with recently reported numbers for NbN-SNSPDs on SiN-waveguides operated at lower temperatures, some of which used very significantly longer nanowires, consequently featuring higher absorption efficiency and slower detector speeds.[46] Notable shorter decay times have been achieved with photonic crystal cavity integrated SNSPDs, however, at the expense of lower on-chip detection efficiencies and optical bandwidth limitations, as compared to our device.[39,48] The dark count rate of our devices were only assessed under daylight operating conditions, indicating no serious performance limitations, although somewhat exceeding record low numbers reported for ultra-short, resonator-integrated SNSPDs[39] and NbTiN-SNSPDs.[44] Implementing an additional series inductor, the latter NbTiN-SNSPD on the SiN-waveguide material combination has also recently led to the demonstration of jitter values around 20 ps,[47] which our detectors exceed due to their lower signal-to-noise ratio owing to operation close to the critical temperature. Finally, our MoSi-nanowire device, fabricated in electron beam lithography, can be operated at significantly higher temperatures than similar WSi-devices fabricated using photolithography on an i-line stepper.[32] Overall, it is apparent that there are trade-offs between these performance characteristics and particular design choices allow for optimal performance in one figure of merit at the expense of another, which may nevertheless benefit more specialized applications. While our first realization of a waveguide-integrated SNSPD with an amorphous material system already achieves all-around performance comparable to significantly further advanced (poly-)crystalline waveguide-integrated SNSPDs, improvements in the electrical readout circuit, stray light suppression, or integration with sophisticated nanophotonic cavities will likely allow for refining all relevant benchmarks.

In conclusion, we have shown that amorphous nanowires can be integrated with nanophotonic circuits and allow for realizing excellent single-photon detection performance at 2.1 K. Employing a novel nanofabrication process for waveguide-integrated MoSi-SNSPDs, we achieve saturated on-chip detection efficiency of (73 ± 10) % for telecom wavelength photons in photonic integrated circuits. Our SNSPD design also allows for high counting rates, accurate timing, and sub-10 Hz dark count rate within the range of saturated detection efficiency. The 4.6 ns output pulse decay time enables fast single-photon counting applications as desired, for example, in quantum communication protocols. Jitter values below 150 ps using electrical amplification at room-temperature are comparable to similar conventional SNSPDs[19] and promise significantly better timing accuracy with cryogenic amplification.[25] While our devices show good all-around performance, it is possible to trade the detector recovery time for on-chip detection efficiency, i.e., one may choose to fabricate longer nanowires, yielding higher OCDE but longer dead time. We also show that these attractive performance characteristics are achieved with common nanophotonic circuit components, which highlights the potential of amorphous superconductors for integrated quantum technology.[49] Our results pave the way for assessing the device yield and more challenging substrate material systems of optimized devices in future work with photonic integrated circuits. We expect that applications requiring large numbers of detectors or more involved substrate material systems will benefit from amorphous waveguide-integrated SNSPDs.

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DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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