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Computing with volatile memristors: an application of non-pinched hysteresis

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Abstract

The possibility of in-memory computing with volatile memristive devices, namely, memristors requiring a power source to sustain their memory, is demonstrated theoretically. We have adopted a hysteretic graphene-based field emission structure as a prototype of a volatile memristor, which is characterized by a non-pinched hysteresis loop. A memristive model of the structure is developed and used to simulate a polymorphic circuit implementing stateful logic gates, such as the material implication. Specific regions of parameter space realizing useful logic functions are identified. Our results are applicable to other realizations of volatile memory devices, such as certain NEMS switches.

Keywords: memristor, in-memory computing, material implication, field emission, graphene

(Some figures may appear in colour only in the online journal)

1. Introduction

Currently, there is strong interest in the in-memory computing concept. In particular, there are expectations that in-memory computing architectures may help to overcome the von Neumann bottleneck problem [1] of conventional computers and thus provide us with better computing machines. Memristive [2] (memory resistive) and memcapacitive [3] (memory capacitive) elements that combine information processing and storage functionalities in simple device structures of nanoscale dimensions have received a great deal of attention in the context of an in-memory computing (memcomputing [4]) paradigm. In fact, the material implication gate was demonstrated experimentally with non-volatile memristive devices several years ago [5]. This idea has been further developed and reviewed in a number of papers [6–12].

While there is a wide variety of physical systems with memory [13], it is generally agreed that non-volatile memory devices are the most suitable candidates for in-memory computing, and for good reason. In this paper, however, we explore a different route to in-memory computing based on *volatile* memristive devices. It is shown that, in principle, simple circuits of volatile memristors can provide some useful logic functions. Here, we do not aim to develop a practical in-memory computing architecture, but rather present a proof of concept application of volatile memristors. Eventually, it may find its own application niche.

To make our description physically based, in this paper we consider the hysteretic behavior of carbon-based field emitters [14–18]. For concreteness, we have chosen a hysteretic graphene-based field emission structure [17] as a prototype of a volatile memristor. The memory effect in such a structure is attributed to a field-induced detachment of a portion of a graphene sheet from a substrate [17]. As in this system, the minimum voltage required to induce an OFF to ON transition V_{ON} is larger than that needed for the transition from ON to OFF, V_{OFF}, there is a voltage interval where the structure remembers its state (defined by the history of the voltage applied). The choice of the graphene-based moving emitter is justified by the combination of its unique electrical and mechanical properties [19] potentially viable for long-time operations [20].

Thus, there are two main results reported in this paper: (i) the memristive model of graphene field emitters, and (ii) realization of in-memory computing gates based on such devices. Accordingly, this paper is organized as follows. We

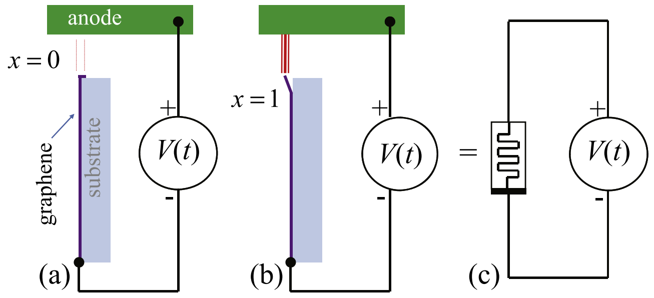

Figure 1. (a) and (b): schematic representation of low- and high-current states of the graphene field emitter: (a) the low-current state (the edge is attached to the substrate, $x = 0$) and (b) the high-current state (the edge is detached/standing, $x = 1$). Both states are stable at $V_{OFF} < V < V_{ON}$. (c) Memristive circuit model of the circuits in (a) and (b).

develop a memristive model of hysteretic graphene-based field emitters in section 2. In particular, in the first part of this section, we formulate general equations of the model, while in the second part (that may be skipped by those readers who are not interested in model details), we formulate the model parameters based on our understanding of physical processes associated with graphene detachment from a substrate. In section 3, an implementation of logic gates based on volatile memristors is explored. We conclude in section 4 with a summary of our study.

2. Memristive model of graphene field emitters

In this section we develop a memristive model of graphene field emitters [17] showing that such devices can be classified as first-order voltage-controlled memristive systems. Our model is well suited for the description of experimental results as it captures both the switching dynamics and physics of field emission. We emphasize that the suggested memristive model can be adopted for the description of other nano-mechanical systems with memory, including those [21–23] that do not require high voltages for their operation. The switching voltages for such two-terminal NEMS switches are below 10 V [21, 22], making them potentially compatible with CMOS logic signals. We emphasise that the stateful logic with NEMS introduced in this work is fundamentally different from previously considered NEMS logic designs [24].

2.1. Memristive model

In a recent experiment [17], a strong hysteresis in current–voltage characteristics of field emission from the edge of graphene on SiO_2 was observed. This behavior was explained by a field-assisted local detachment of the graphene edge from the substrate (for a schematic illustration see figure 1). In particular, it was demonstrated that when the system is subjected to an increasing voltage V from 0 to a maximum value, there is a rapid increase in the current at a certain V_{switch} (in what follows, denoted by V_{ON}). On the way back, a current drop is observed at $V_{OFF} < V_{ON}$ such that $V_{ON}/V_{OFF} \approx 7$. Importantly, in the hysteretic region (ranging from V_{OFF} to V_{ON}), the current is stable in the sense that the system can stay arbitrarily long in one of two (in some samples, many) possible current states. Thus, the memory of such field emitters can be classified as long-term and volatile (the memory is lost at small V including $V = 0$).

In order to describe the hysteretic field emission from graphene, we use the formalism of memristive devices developed by Chua and Kang [2]. According to the definition, an N-order voltage-controlled memristive system is given by

$$I(t) = R_M^{-1}(\mathbf{x}, V, t)V(t), \tag{1}$$
$$\dot{\mathbf{x}} = f(\mathbf{x}, V, t), \tag{2}$$

where R_M is the memristance (memory resistance), which depends on the input voltage V and vector $\mathbf{x}$ of N internal state variables. The function f in equation (2) defines the dynamics of the internal state. Nowadays, equations (1)–(2) are widely used to model a broad range of emergent non-volatile memory devices [13]. Moreover, the present authors applied equations (1)–(2) to field emission from carbon nanotubes [18].

It is natural to select the internal state variable x as $x = L_p/L_{tot}$, where L_p is the length of the detached (standing) portion of the edge, and L_{tot} is the edge length. Two limit cases (completely attached, $x = 0$, and detached, $x = 1$, edges) are schematically depicted in figure 1. Generally, x can take any intermediate value between 0 and 1. To formulate the memristive model of graphene field emitters, we assume that the current in $x = 0$ and $x = 1$ states can be described by the Fowler–Nordheim law [25]. Note that this assumption is in agreement with experimental observations [17].

The total current can be written as a sum of currents through the attached and detached regions of the edge:

$$I = (1 - x)I_{OFF} + xI_{ON}, \tag{3}$$

where I_{OFF} and I_{ON} are the total emission currents at $x = 0$ and $x = 1$, respectively. I_{OFF} and I_{ON} are represented using the Fowler–Nordheim law as

$$I_{OFF(ON)} = A_{OFF(ON)} V^2 \exp -\frac{B_{OFF(ON)}}{V}. \tag{4}$$

Here, $A_{OFF(ON)}$ and $B_{OFF(ON)}$ are constants discussed in section 2.2.

In order to reproduce the experimental results [17], it is sufficient to select the function f in equation (2) as

$$f(V) = \begin{cases} \gamma & \text{if } V \geqslant V_{ON} \\ -\gamma & \text{if } V \leqslant V_{OFF}, \\ 0 & \text{otherwise} \end{cases} \tag{5}$$

where $\gamma > 0$ is the rate of change of x. In fact, the function f defined by equation (5) can describe both types of memristors: non-volatile and volatile. Assuming a positive V_{ON}, the memristor type is defined by inequalities

$$\begin{aligned} V_{ON} > V_{OFF} \geqslant 0 &: \text{ volatile}, \\ V_{ON} > 0 > V_{OFF} &: \text{ non-volatile}. \end{aligned} \tag{6}$$

Figure 2 schematically shows examples of the dynamics of x in a volatile memristor (such as the graphene field emitter), figure 2(a), and in a hypothetical non-volatile memristor,

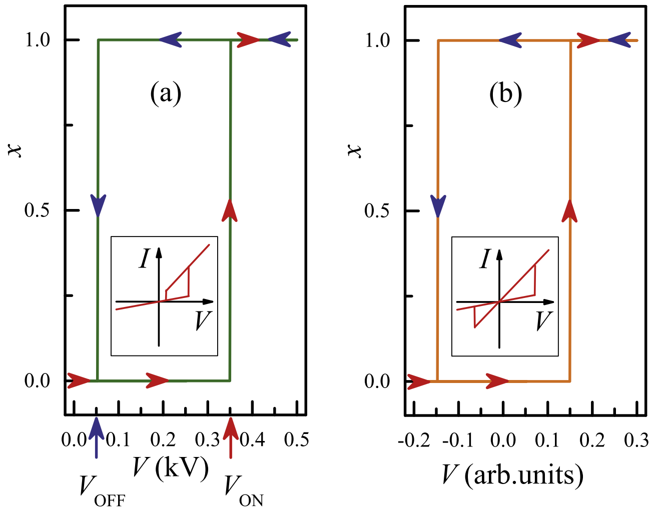

Figure 2. Hysteretic curves for the internal state variable x of (a) volatile (graphene field emitter) and (b) hypothetical nonvolatile memristor. The insets demonstrate respective non-pinched and pinched hysteretic I–V curves.

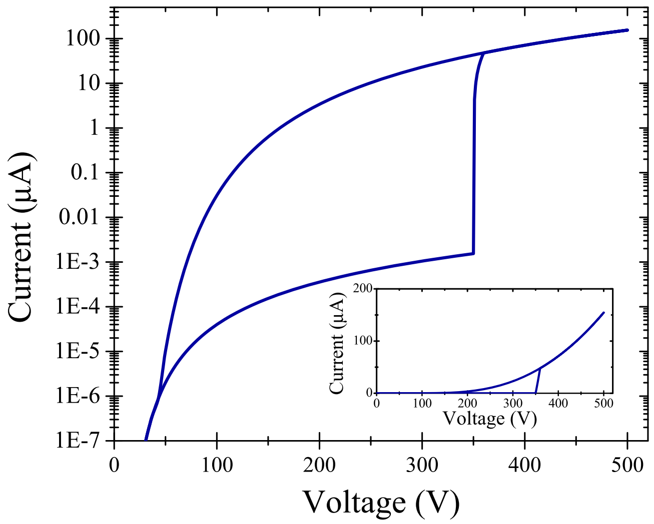

Figure 3. I–V curve of the graphene field emitter found using equations (1)–(5) with the following set of parameter values: $V_{\mathrm{OFF}} = 50$ V, $V_{\mathrm{ON}} = 350$ V, $A_{\mathrm{ON}} = 2.32 \cdot 10^{-9}$ A V^{-2}, $B_{\mathrm{ON}} = 662.2$ V, $A_{\mathrm{OFF}} = 1.99 \cdot 10^{-14}$ A V^{-2}, $B_{\mathrm{OFF}} = 160.6$ V, $\gamma T = 100$, where T is the voltage period. Inset: the same curve shown in the linear scale.

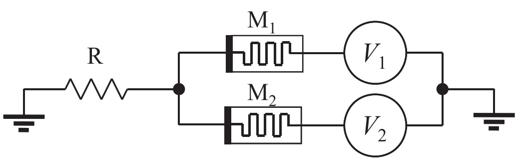

Figure 4. In-memory computing circuit considered in this work. The circuit combines two memristors M_i, resistor R and two voltage sources.

figure 2(b), subjected to a periodic quasistatic waveform voltage.

A calculated I–V curve of a graphene field emitter subjected to a triangular waveform voltage is shown in figure 3.

Table 1. Codes [12] of logic operations calculated according to equation (9). These codes are defined with respect to different pairs of initial states of M_1 and M_2 and can describe the final state of any device of interest (in our case, M_1 or M_2). For more information, see the text and [12].

Set to 0	0	XOR	6	copy M_1	12
NOR	1	NAND	7	IMP_2	13
NOT(IMP_2)	2	AND	8	OR	14
NOT M_1	3	NOT(XOR)	9	set to 1	15
NOT(IMP_1)	4	copy M_2	10		
NOT M_2	5	IMP_1	11		

We emphasize that our volatile memristor exhibits a non-pinched hysteresis.

2.2. Physical basis of the model

Here, we briefly discuss the expressions for the model parameters $A_{\mathrm{OFF(ON)}}$ and $B_{\mathrm{OFF(ON)}}$.

Consider the field emission from a graphene-based cathode, as presented in figure 1. The potential difference $V(t)$ between the cathode and anode results in the electric field $E = \beta V/D$, where D is the distance between the electrodes and β is the form factor. Then the current is described by the Fowler–Nordheim formula [14, 26]

$$I(V) = AV^2 \exp(-B/V),$$
$$A = \frac{e^3}{16\pi^2\hbar}\frac{1}{\varphi}\left(\frac{\beta}{D}\right)^2 S, \quad B = \frac{4\sqrt{2m}}{3e\hbar}\varphi^{3/2}\left(\frac{\beta}{D}\right)^{-1}, \tag{7}$$

where e and m are the electron charge and mass, $\hbar$ is the Planck constant, S is the effective emitting surface, and $\varphi = 4.8$ eV is the work function.

In figure 1, situation (a) corresponds to the graphene sheet entirely attached to the substrate, while in case (b), the edge of the sheet is detached. Following the arguments put forward in [17], we believe that the main effect is likely associated with the change in the form factor β and effective emitting surface S. Introducing $\beta_{\mathrm{OFF(ON)}}$ and $S_{\mathrm{OFF(ON)}}$ for the low- and high-current states, the model parameters are defined as $A_{\mathrm{OFF(ON)}} \equiv A(S_{\mathrm{OFF(ON)}}, \beta_{\mathrm{OFF(ON)}})$ and $B_{\mathrm{OFF(ON)}} \equiv B(S_{\mathrm{OFF(ON)}}, \beta_{\mathrm{OFF(ON)}})$. An intermediate situation is described by the superposition state, equation (3).

3. Logic gates

3.1. Circuit and calculation of the operation code

The possibility of in-memory computing with volatile memristors is investigated employing the circuit shown in figure 4, which is similar to the circuit used in the demonstration of the material implication with non-volatile memristors [5]. In what follows, this circuit is simulated based on the Kirchhoff's

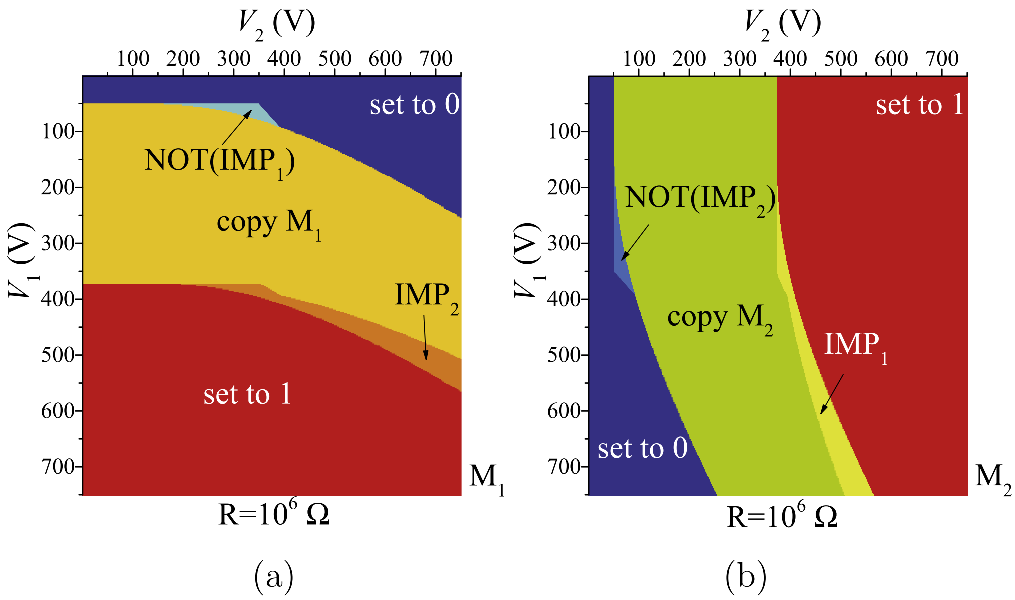

Figure 5. Operation type as a function of applied voltages calculated using the figure 4 circuit with $R = 10^6\ \Omega$. The final states of M_1 and M_2 hold the logic function outputs presented in (a) and (b), respectively. These plots were obtained with the same parameters of M_1 and M_2 as in figure 3.

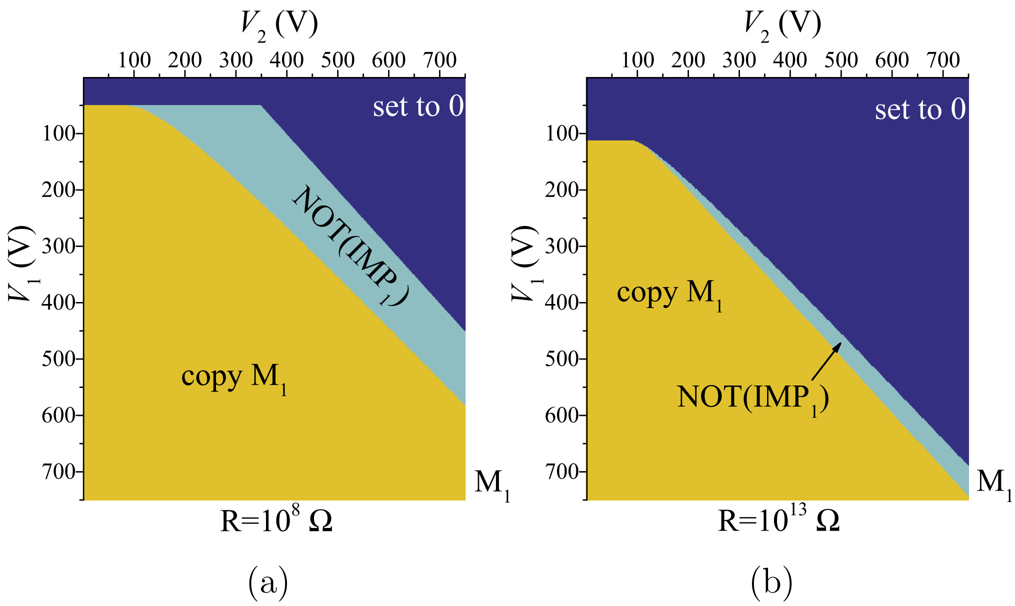

Figure 6. Operation type as a function of applied voltages calculated using the figure 4 circuit with $R = 10^8\ \Omega$ and $10^{13}\ \Omega$. These plots were obtained with the same parameters of M_1 and M_2 as in figure 3.

circuit laws equation for $V_R(t)$

$$\frac{V_1 - V_R(t)}{R_{M,1}} + \frac{V_2 - V_R(t)}{R_{M,2}} = \frac{V_R(t)}{R}, \tag{8}$$

which is supplemented by equations (1), (2) for the dynamics of memristances $R_{M,1}$ and $R_{M,2}$. In equation (8), $V_R(t)$ is the voltage across R.

Following [12], we analyze the simulation results calculating a numerical code that can be associated with a specific logic operation. Taking $w_i = 1, 2, 4, 8$ as weights for the input combinations (0, 0), (0, 1), (1, 0) and (1, 1), the numerical code is calculated as a weighted sum of the final state of a selected memristor,

$$\text{code} = \sum_{i=1}^{4} w_i b_{ij}^f, \tag{9}$$

where b_{ij}^f is the final state (0 or 1) of the device of interest j (in our case, M_1 or M_2) for the ith input combination (0, 0), (0, 1), (1, 0) or (1, 1) that corresponds to $i = 1, 2, 3, 4$. Table 1 summarizes the logic functions for all possible code values. In this table, the standard notations are used for the logic functions, e.g. NOT is the logical negation, IMP is the material implication (in particular, IMP_1 is $M_1 \rightarrow M_2$), etc. In

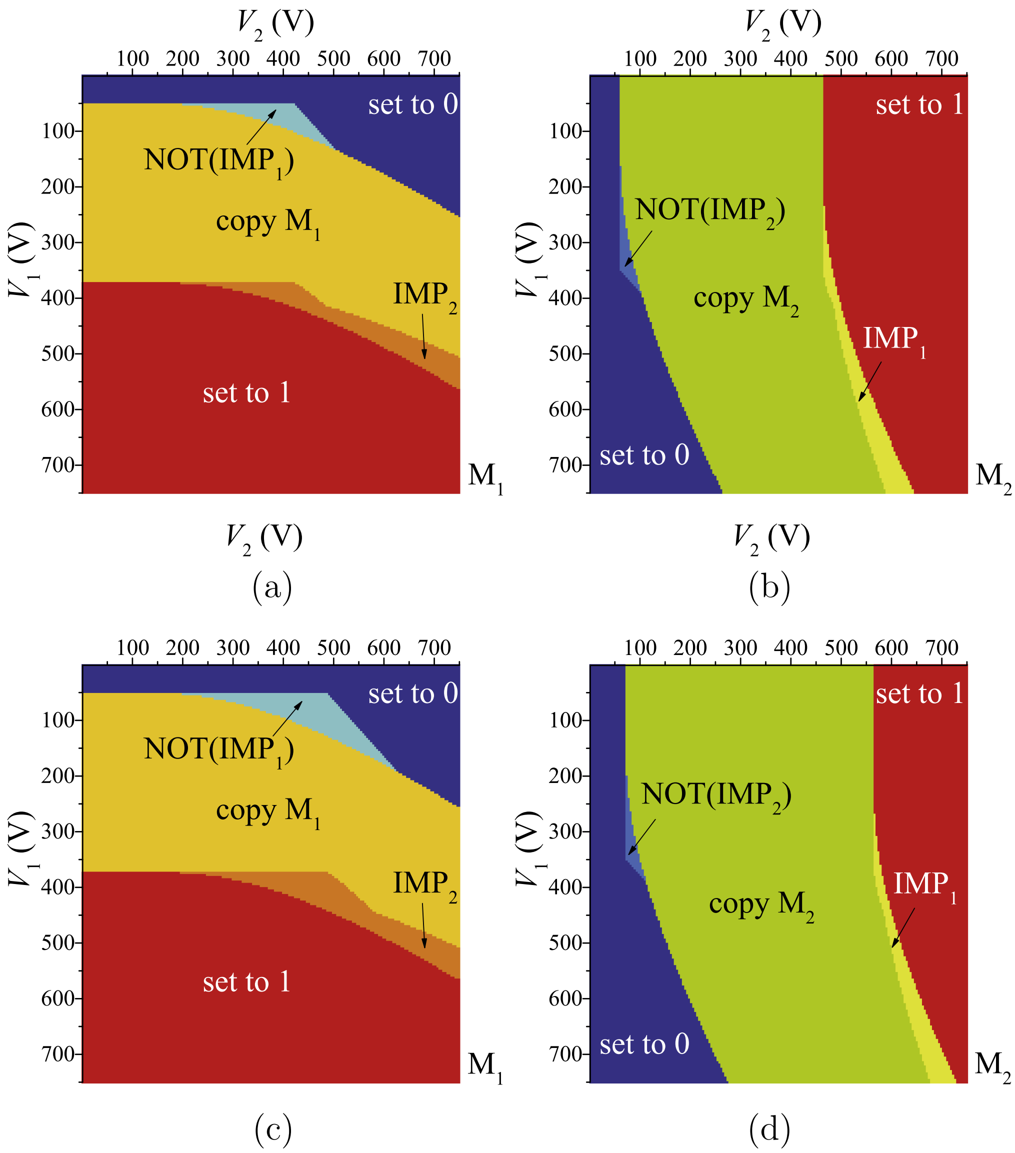

Figure 7. Effect of the variability of memristor parameters. To obtain these plots we used $R = 10^6\ \Omega$, and higher $V_{\mathrm{ON(OFF)}}$ for M_2: $V_{\mathrm{OFF}} = 60$ V and $V_{\mathrm{ON}} = 420$ V in (a) and (b), and $V_{\mathrm{OFF}} = 70$ V and $V_{\mathrm{ON}} = 490$ V in (c) and (d). All other model parameters are as per figure 3. Compare with figure 5.

our numerical simulations of the figure 4 circuit, we have encountered the following operation codes: 0, 2, 4, 10–13, 15.

3.2. Diagrams of logic operations

Figures 5 and 6 show some selected results of our simulations. In order to obtain each point of these plots, we simulated the dynamics of the figure 4 circuit for all possible pairs of the initial states of M_1 and M_2 subjected to V_1 and V_2. The operation code was found with equation (9) and interpreted based on table 1.

According to figure 5, the logic operations are symmetric for M_1 and M_2 with respect to the $V_1 = V_2$ line. As expected, at low voltages applied to M_i, x_i changes to 0, and at high voltages, it changes to 1, and there is also a stability region (copy to M_i). At $R = 0$, the common stability region is a square defined by the lines $V_i = V_{\mathrm{ON(OFF)}}$. This square is deformed at $R > 0$ (this can be seen by placing figure 5(b) over figure 5(a) or vice versa). The most important voltages regions, however, are those providing the material implication (IMP) and negation of implication (NOT(IMP)) gates. The importance of the material implication stems from the fact that it is a fundamental logic gate [27], which, together with 'set to 0' (FALSE) operation, form a computationally complete logic basis.

Figure 6 shows the effect of the resistance of R on logic operations regions. One can notice that, generally, an increase in R scales the operation regions in figure 5(a) to higher voltages. In particular, one can notice the disappearance of 'set to 1' regions (these regions are now beyond the scales presented) and, in fact, an increase of the region of NOT (IMP). This observation, actually, is of value as the proper choice of R simplifies the experimental realization of logic gates and improves reliability.

In order to demonstrate the proposed logic gates experimentally, one can implement, for example, the following operation protocol. First of all, the memristors can be independently initialized by grounding the common point of their connection with R and applying suitable voltage sequences $V_1(t)$ and $V_2(t)$. Next, the grounding of the connection point is released while V_1 and V_2 are kept in the stability region of memristors (operation codes 10 and 12). Third, V_1 and V_2 can be simultaneously placed into the desired operation point and switched back into the stability region. The calculation results will be stored in the final states of the memristors.

3.3. Parameter variability effects

In this section, we investigate the effect of the variability of memristor parameters on the logic functions realized with the figure 4 circuit. Specifically, we consider the operation of the figure 4 circuit employing memristors with different threshold voltages. For this purpose, the simulations are performed using higher values of threshold voltages of M_2, keeping all other simulation parameters as in the figure 5 simulations. Figure 7 presents two examples of such calculations showing the diagrams found at about 20% and 40% higher threshold voltages of M_2 compared to M_1.

In figure 7, one can notice that the diagrams for M_1 and M_2 are no longer symmetric. At the same time, the general topologies of the diagrams are the same as those in figure 5. Importantly, the areas of useful logic functions for M_1 (the implication and negation of implication) increase with an increase in V_{OFF} and V_{ON} of M_2. This observation can be used, e.g. to achieve more stable operation of such memristive logic gates.

4. Conclusion

We considered the possibility of in-memory computing (in the form of boolean logic) based on volatile memristive devices. As a prototype of such structures, a hysteretic graphene field emitter was adopted. A memristive model of field emission from the graphene cathode was developed. This model is practical for the description of real experiments. While the hysteretic graphene field emitter considered in this work requires high voltages for its operation (hundreds of volts), its switching voltages can be reduced down to a few tens of volts [28] reducing the gap between the electrodes. Two-terminal NEMS switches [21–23] provide a low-voltage alternative to high-voltage hysteretic graphene field-emission devices.

Moreover, it was shown that simple circuits of volatile memristors can serve as a polymorphic logic gate. Specifically, we have demonstrated that in addition to the trivial operation set (FALSE, TRUE and hold the state), the same circuit can implement the material implication and the negation of implication. We expect that volatile memristors could find their own applications, e.g. in low-level information processing circuits.

Acknowledgments

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